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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,753	06/07/2001	Sam Gat-Shang Chu	YOR9-2001-0127US1 (8728-	1871

7590

05/18/2004

Frank Chau, Esq.
F. CHAU & ASSOCIATES, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

EXAMINER

TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/876,753

Applicant(s)

CHU ET AL.

Examiner

John J Tabone, Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 12-18 is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

1. The pending claims 1-17 and new claim 18 have been examined.

Claim Objections

2. Claim 17 is objected to because of the following informalities: On line 3 predetermined is misspelled. "Predetermeined" should be "predetermined". Appropriate correction is required.
3. Claim 18 is objected to because of the following informalities: On lines 5 and 12 "over riding" and "over ride" should be changed to "overriding" and "override", respectively.

Response to Amendment

Drawings

4. The proposed drawing corrections have been received on 03/09/04 and are corrected for consistency with specification. The objections per paper 3, ¶s 2 and 3 are withdrawn.

Specification

5. The specification objection for consistency with Figure 6 has been amended. The objection per paper 3, ¶ 4 is withdrawn.

Claim Rejections - 35 USC § 112

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6. The rejections of claim 1-12, 14, 16, and 17 under 35 U.S.C. 112, second paragraph, in paper 3, ¶ 5 have been overcome by the Applicant by amending claims 1-7, 12, 14, 16 and 17. The rejections have been withdrawn.

Response to Arguments

7. Applicant's arguments, see Remarks, filed 3/9/04, with respect to the rejection(s) of claim(s) 1-17 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection of claims 1-3, 5-7, 9 and 11 are made in view of Rajski et al. (US-5991909).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8 and 10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8:

This claim recite the limitation "wherein the control unit includes an OR gate". The word "includes" is an all-inclusive word and does not define what else is part of the control unit. The specification on page 11, line 18 recite "A control unit 54, which can be an OR gate. Also, figure 6 shows the control unit 54 as an OR gate. It is suggested to

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overcome this rejection claim 8 should be rewritten to recite "wherein the control unit is an OR gate".

Claims 10:

This claim recite the limitation "wherein the masking unit includes an AND gate". The word "includes" is an all-inclusive word and does not define what else is part of the masking unit. The specification on page 11, line 21 recite "A masking unit 56, which can be an AND gate. Also, figure 6 shows the control unit 56 as an AND gate. It is suggested to overcome this rejection claim 10 should be rewritten to recite "wherein the masking unit is an AND gate".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 5-7, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajski et al. (US-5991909).

Claim 1, 2 and 11:

Rajski teaches a parallel decompressor 10 also includes multiplexors 24 (loading unit) for selecting either a test data input bit (TDI) (masking data) or a feedback data bit for LFSR 12 (masking register file). Rajski teaches a MISR 28 for receiving signatures. (See Fig. 1). Rajski also teaches a multiplexor 26 (masking unit) for

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selecting the output data bits of LFSR 12 (masking data) or data bits being shifted from one flip-flop chain 15 to another flip-flop chain (scanning data from a scan string). (See col. 5, lines 54-59).

Claim 3:

Rajski teaches the number of scan flip-flops used by the decompression structure was selected such that the total number of flip-flops in the decompressor is greater than $S_{\max} + 20$, where S_{\max} is the maximum number of specified positions in any test cube (scan string). (Col. 6, lines 38-42).

Claim 5 and 7:

Rajski teaches the parallel decompressor 10 also includes AND gates 20 (control unit) for overwriting the data bits (controls the masking register to withhold the masking data) being shifted from one flip-flop chain 15 to another flip-flop chain 15, to allow constant zeroes (predetermined value, claim 9) to be provided to all or selected positions of each of flip-flop chains 15 (testing of a predetermined latch, claim 5). (Col. 5, lines 55-65, Fig. 1).

Claim 6:

Rajski discloses in claim 22(d), repeatedly applying clock cycles to shift the contents of the LFSR and the scan chains, until all flip-flops of the scan chains are filled with output data bits from the LFSR. By this Rajski teaches that the LFSR 12 (masking register file) and the scan chains (latches in the scan string) are shifted bit-by-bit synchronously to a clock.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al. (US-5991909) in view of Kim (US-5574733).

Claim 4:

Rajski does not explicitly teach the LFSR includes a scan-only register, however, Rajski does teach the parallel decompressor 10 includes LFSR 12 (masking register file) and multiple pluralities of serially connected flip-flops or flip-flop chains. (Col. 5, lines 32, 34). Kim teaches the LFSR comprises a chain of scan flip-flops 210-213. (Col. 2, lines 21-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rajski's LFSR 12 to include Kim's scan flip-flops. The artisan would be motivated to do so because it would enable would Rajski's LFSR 12 (masking register file) to be tested as part of the multiple scan chains and also shift the masking data from the TDI input or the feedback data bit through multiplexer 24 (loading unit).

Allowable Subject Matter

11. Claims 12-18 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The prior art of record teaches a test unit, a loading unit, which is a multiplexor, a masking unit a masking register file and a control unit. Also, the prior art of record teaches the overriding of data bits to selected positions of each flip-flop chain (predetermined latch); Rajski et al. (US-5991909) is one example of such prior arts. As per claims 8 and 10, the prior arts of record, however, fail to teach, singly or in combination, the masking unit being an AND gate, and the control unit being an OR gate. Claims 8 and 10 would be allowed if the rejections under 35 U.S.C. 112, second paragraph are overcome. The Examiner asserts that the novelty of the claim, when read as a whole, is the device for fault testing wherein a testing unit has a reference signature indicative of faults at a particular frequency. A masking unit, which is an AND gate, generates a signature based on masking and scanning data received from a loading unit and a scan string in the chip respectively. The control unit, which is an OR gate, controls the output of the masking register file, to withhold the making data.

As per claims 12-18, the prior arts of record, however, fail to teach, singly or in combination, Loading a masking data set through the loading unit (MUX) indicative of the known latch failure pattern; overriding use of the masking data set via the control unit (OR gate) for determining the reduced failing frequency a portion of the chip; generating a first reference signature indicative of the faults of the portion of the chip at the reduced failing frequency and testing that signature against a target signature; identifying a failing pattern if the reference signature is not equal to the target signature; then removing the override to allow use of the masking data set, masking the failing patterns; scanning data from a scan string in the chip and replacing the first reference

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signature with the resulting signature generated by the masking data set. Also, by replacing the signatures, the test is continued at higher frequencies, therefore the failure of the test is prevented. The Examiner agrees with the applicants arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of claims 12-18.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

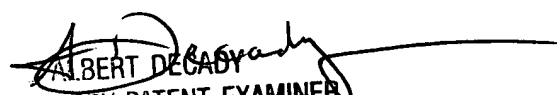
Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT



ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100